What is claimed is:

1. A digital system comprising:

a master circuit, which includes a circuit to detect clock delay, receives a system reset signal, and generates output data, an output clock signal with which the output data is synchronized, and a reset control signal which responds to the system reset signal; and

a slave circuit in signal communication with the master circuit, where the slave circuit is reset in response to a reset control signal, receives the output clock signal and the output data, and sends to the master circuit an input clock signal as a feedback signal of the output clock signal and input data that is synchronized with the input clock signal,

wherein the circuit to detect clock delay generates the reset control signal in response to the system reset signal or an internal reset signal, detects a delay between the output clock signal and the input clock signal, and loads and unloads the input data in response to an initial parameter corresponding to the delay.

2. The digital system of Claim 1, wherein the internal reset signal is a clock signal generated when detected delays are not identical to one another.

3. A circuit to detect clock delay comprising:

a delay detection circuit, which detects a delay between an output clock signal and an input clock signal, generates an initial parameter corresponding to the delay if detected delays are identical to one another or continuously detects the delays until the detected delays are identical to one another if detected delays are not identical to one another, and generates a reset control signal in response to a system reset signal or an internal reset signal; and

a clock forwarding circuit in signal communication with the delay detection circuit, where the clock forwarding circuit loads and unloads input data in response to the initial parameter.

4. The circuit of Claim 3, wherein the delay detection circuit further comprises:

a detection circuit, which is used to detect a delay between the output clock signal and the input clock signal;

a comparison circuit in signal communication with the detection circuit, which compares the detected delays and generates the initial parameter when the detected delays are identical to one another; and

a control circuit in signal communication with the comparison circuit, where if detected delays are not identical to one another, resets the detection circuit, generates the reset control signal in response to the internal reset signal, and controls the

comparison circuit to perform a comparison operation by N-bit free running until all the detected delays are identical to one another.

5. The circuit of Claim 4, wherein the detection circuit comprises:

a counting unit, which includes two D-type flip flops that are synchronized with the output clock signal and are reset by the input clock signal; and

a detection unit in signal communication with the counting unit, which receives output of the counting unit and detects the delay between the output clock signal and the input clock signal in response to the input clock signal.

6. The circuit of Claim 4, wherein the comparison circuit further comprises:

a latch unit, which includes a demultiplexer and N latches, respectively latches most significant bits and least significant bits of the delays outputted from the detection unit by N-bit free running; and

a comparison unit in signal communication with the latch unit, which compares the most significant bits and least significant bits outputted from the latch unit, outputs one of the most significant bits and one of the least significant bits as the initial parameters, and outputs a first signal at a first level if all most significant bits and least significant bits are respectively identical to one another, or outputs the first signal at a second level if all most significant bits and least significant bits are not respectively identical to one another.

7. The circuit of Claim 6, wherein the control circuit comprises:

an N-bit free running counter/decoder, which controls the demultiplexer to perform N-bit free running in response to the first signal and sends a predetermined clock signal to the latch unit;

a system clock control unit in signal communication with the counter/decoder, which receives the clock signal in response to the first signal and outputs the clock signal as an internal reset signal; and

a reset control unit in signal communication with the system clock control unit, which receives the system reset signal or the internal reset signal, sends the received system reset signal or internal reset signal to the N-bit free running counter/decoder, resets the detection unit, and outputs the system reset signal or the internal reset signal as the reset control signal.

8. The circuit of Claim 7, wherein the clock forwarding circuit comprises:

a clock generator, which is reset in response to output of the system clock control unit and generates the clock signal;

an internal data bus in signal communication with the clock generator, which is used for data interface with a predetermined master circuit;

a data control unit in signal communication with the internal data bus, which is connected to the internal data bus and outputs data to a slave circuit in response to the clock signal;

an output clock signal control unit in signal communication with the internal data bus, which outputs the output clock signal to the slave circuit in response to the clock signal;

an input clock signal control unit in signal communication with the internal data bus, which receives and controls the clock signal and outputs the controlled clock signal;

a load/unload clock control unit in signal communication with the internal data bus, which receives the controlled clock signal and generates load control signals and unload control signals in response to the initial parameter; and

a load/unload multiplexer in signal communication with the internal data bus, which receives input data inputted from the slave circuit and unloads the input data to the internal data bus, through the data control unit, in response to the load control signals and the unload control signals.

9. The circuit of Claim 8, wherein the output clock signal is a signal outputted from a predetermined master circuit, the input clock signal is a signal outputted from a predetermined slave circuit, and the input clock signal is a feedback clock of the output clock signal.

10. The circuit of Claim 3, wherein the internal reset signal is a clock signal generated when one of the detected delays is not identical to other detected delays.

11. The circuit of Claim 3, wherein the reset control signal is generated when the system reset signal or the internal reset signal is activated.

12. A method of detecting clock delay comprising:

(a) detecting a delay between an output clock signal and an input clock signal and generating an initial parameter corresponding to the delay if the detected delays are identical to one another;

(b) continuously detecting the delay until the detected delays are identical to one another and generating a reset control signal in response to the system reset signal or the internal reset signal, if the detected delays are not identical to one another; and

(c) loading and unloading input data in response to the initial parameter.

13. The method of Claim 12, wherein step (a) further comprises:

(a1) detecting and outputting a delay between the output clock signal and the input clock signal;

(a2) respectively latching most significant bits and least significant bits of the delays outputted in step (a1); and

(a3) comparing the most significant bits and the least significant bits outputted in step (a2), outputting one of the most significant bits and one of the least significant bits as the initial parameters, and outputting a first signal at a first level if all most significant bits and least significant bits are respectively identical to one another, or outputting the first signal at a second level if all most significant bits and least significant bits are not respectively identical to one another.

14. The method of Claim 13, wherein step (b) is characterized by generating the reset control signal for resuming step (a) in response to the first signal if one of the detected delays is not identical to other detected delays and resuming step (a) by N-bit free running until the detected delays are identical to one another.

15. The method of Claim 14, wherein step (b) further comprises:

(b1) generating an internal reset signal in response to the first signal and a predetermined clock signal;

(b2) receiving the system reset signal or the internal reset signal, and generating the reset control signal; and

(b3) performing N-bit free running in response to the first signal and generating an N-bit free running signal.

16. The method of Claim 15, wherein step (c) further comprises:

(c1) generating the clock signal;

(c2) outputting the output clock signal to a slave circuit in response to the clock signal;

(c3) receiving and controlling the clock signal, and outputting the controlled clock signal;

(c4) receiving the controlled clock signal, and generating load control signals and unload control signals in response to the initial parameter; and

(c5) receiving input data inputted from the slave circuit, and unloading the input data in response to the load control signals and the unload control signals.

17. The method of Claim 12, wherein the output clock signal is outputted from a predetermined master circuit, the input clock signal is outputted from a predetermined slave circuit, and the input clock signal is a feedback clock of the output clock signal.

18. The method of Claim 12, wherein the internal reset signal is generated when the detected delays are not identical to one another.

19. The method of Claim 12, wherein the reset control signal is generated when the system reset signal or the internal reset signal is activated.

20. A circuit to detect clock delay as defined in Claim 3, the circuit further comprising:

detection means for detecting successive delays between an output clock signal and an input clock signal; and

reset means for comparing the detected successive delays between the output clock signal and the input clock signal, generating an initial parameter responsive to at least one of the delays and generating an internal reset signal if the detected delays are not similar to each another, and generating an initial parameter responsive to an approximated delay and generating a reset control signal in response to the system reset signal if the detected delays are similar to each another.